REMARKS

Favorable reconsideration of this application in view of the remarks to follow is respectfully requested.

Before addressing the specific grounds of rejection, applicants have provided formal drawings, added new Claim 72, and amended Claim 30.

The formal drawings, which are enclosed with this response, attend to the requirement that the applicants comply with 37 C.F.R. §1.84(L).

Applicants have amended Claim 30 to more clearly and positively recite applicants' field effect transistor. Support for amended Claim 30 is found throughout applicants' specification. See, for example, Page 12, lines 3-17, and Figs. 13-16. Referring to FIG. 16, amended Claim 30 recites a field effect transistor comprising a substrate 12 of a single crystal semiconducting material, two spaced apart metal semiconductor compound regions 40 forming a source and drain and defining a channel there between, a first dielectric layer 18 on said two spaced apart metal semiconductor compound regions 40, a gate dielectric layer 50 of locally reacted metal of said metal used in said metal-semiconductor compound regions 40 on said channel located beneath said two spaced apart metal semiconductor compound regions 40, and a conductive layer 30, 32 on said first dielectric layer 18 and in contact with said gate dielectric layer 50 to form a gate, wherein said first dielectric layer 18 extends under sidewalls of said conductive layer 30,32. Amended Claim 30 is clearly supported by applicants' specification.

Newly added Claim 72 positively and clearly recites a field effect transistor comprising a metal layer 16 atop a substrate 12, the metal layer 16 comprising metal semiconductor regions adjacent to a locally reacted region 50, where the metal semiconductor regions 40 atop the substrate 12 form source/drain regions; a dielectric layer 18 atop each of the metal semiconductor regions 40; and

a conductive layer 30, 32 on the locally reacted metal 50, wherein the conductive layer 30,32 atop the locally reacted metal 50 form a gate. Support for newly added Claim 72 is found throughout applicants' specification. See, for example, Page 12, lines 3-17, Figs. 13-16, Figs. 23-25, and Pages 7-9 of the previously filed preliminary amendment dated April 17, 2000.

Since each and every limitation recited in newly added Claim 72 is supported by applicants' disclosure, applicants respectfully request that newly added Claim 72 be entered.

Claims 30 and 33 stand rejected under 35 U.S.C. §103(a) as allegedly unpatentable over U.S. Patent No. 5,159,416 to Kudoh ("Kudoh") in view of U.S. Patent No. 4,521,446 to Coleman, et al. ("Coleman, et al").

Applicants respectfully submit that the claims of the present application are not obvious from the disclosures of the combined references, since the applied references do not teach or suggest applicants' claimed device, as recited in amended Claim 30. More specifically, the applied references fail to teach or suggest a field effect transistor comprising a substrate 12 of a single crystal semiconducting material, two spaced apart metal semiconductor compound regions 40 forming a source and drain and defining a channel there between, a first dielectric layer 18 on said two spaced apart metal semiconductor compound regions 40, a gate dielectric layer 50 of locally reacted metal of said metal used in said metal-semiconductor compound regions 40 on said channel located beneath said two spaced apart metal semiconductor compound regions 40, and a conductive layer 30, 32 on said first dielectric layer 18 and in contact with said gate dielectric layer 50 to form a gate, wherein said first dielectric layer 18 extends under sidewalls of said conductive layer 30,32. "To establish a prima facie case of obviousness of a claimed invention all the claimed limitations must be taught or suggested by the prior art". *In re Wilson,* 424 F.2d 1382, 1385, 165 USPQ 44, 496 (CCPA 1970).

The primary reference, Kudoh, spurring the instant §103 rejection fails to teach or suggest a first dielectric layer on metal semiconductor compound regions (source/drain regions), where the first dielectric layer 18 extends under the sidewalls of the conductive layer, as recited in amended Claim 30. Kudoh discloses a number of embodiments of thin film transistors each of which incorporating sidewall spacers. The sidewall spacers disclosed in Kudoh ensure that any dielectric material atop the source and drain are separated from the sidewalls of the gate stack (conductive layer). Therefore, Kudoh fail to disclose where the first dielectric layer 18 extends under the sidewalls of the conductive layer, as recited in amended Claim 30. The embodiments disclosed in Kudoh are now discussed in greater detail.

Kudoh discloses a number of embodiments of thin film transistors in each of which the dielectric layer atop the metal semiconductor compound regions (source/drain regions) is separated from the sidewalls of the conductive layer. Referring to Figs. 1-4 of the Kudoh disclosure, Kudoh clearly depicts sidewall spacers abutting the gate electrode 14 (conductive layer). Applicants submit that the sidewall spacer is necessarily present in Kudoh to prevent shorting between the silicide films 15 and 16 and the gate electrode 14. Referring to Fig. 9 of the Kudoh disclosure, Kudoh clearly depicts that the dielectric 98 atop the source 15 and drain 16 is separated from the gate electrode 14 (conductive layer) by the sidewall spacers. Referring to Figs. 5, and 6, Kudoh also discloses bottom gate structures, in which the gate dielectric 61 is positioned on the sidewalls of the gate conductor 60 (conducive layer). In these embodiments the source 65 and drain 66 are above the gate region 60. Referring now to Fig 10, the sidewalls of the gate conductor 60 (conductive layer) in the bottom gate structures disclosed in Koduh are clearly isolated from the dielectric layer 98 that is positioned atop the source 65 and drain 66 regions. Therefore, Kudoh fails to disclose where a dielectric layer atop the metal semiconductor

compound regions (source/drain) extends under the sidewalls of the conductive layer, as recited in amended Claim 30.

Kudoh also fails to teach or suggest *a gate dielectric layer of locally reacted metal of said metal used in said metal-semiconductor compound regions on said channel*, as recited in amended Claim 30. Kudoh discloses a number of embodiments of thin film transistors each of which fail to disclose *a gate dielectric layer of local reacted metal of said metal used in said metal-semiconductor compound regions on said channel*, where the portions of the metal-semiconductor compound adjacent the channel provide source/drain regions, as recited in amended Claim 30.

Kudoh discloses a number of embodiments of thin film transistors in each of which the dielectric layer atop the metal semiconductor compound regions (source/drain) is separated from the sidewalls of the gate stack (conductive layer). Specifically, referring to Column 3, lines 2-18, Kudoh discloses where the gate dielectric 13, 92, 105, is a gate silicon dioxide film, therefore having a different composition than the titanium silicide source/drain regions 15,16, 95. Additionally, Fig. 9 clearly depicts where the titanium silicide source/drain regions 15, 16, 95 and the gate dielectric 13, 92 are formed in different layers of the multilayer structure. Therefore, since Kudoh discloses that the gate dielectric layer and the source/drain regions are different materials positioned in separate and different layers, Kudoh fails to teach or suggest a field effect transistor comprising *a gate dielectric layer of locally reacted metal of said metal used in said metal-semiconductor compound regions on said channel*, as recited in amended Claim 30.

The applied secondary reference, i.e., Coleman, et al., does not alleviate the above mentioned defects in Kudoh, since Coleman, et al. also do not teach or suggest applicants'

claimed field effect transistor. Coleman, et al. disclose a method for depositing polysilicon atop TiO_2, which includes anneal processing steps. Coleman, et al. do not disclose field effect transistors or forming field effect transistors comprising a first dielectric layer on metal semiconductor compound regions (source/drains), where the first dielectric layer extends under the sidewalls of the conductive layer, as recited in amended Claim 30. Coleman, et al. also fail to disclose field effect transistors or forming field effect transistors comprising *a gate dielectric layer of locally reacted metal of said metal used in said metal-semiconductor compound regions on said channel*. Therefore, Coleman, et al. fail to teach or suggest applicants' claimed structure, as recited in amended Claim 30.

The §103 rejection also fails because there is no motivation in the applied references which suggests modifying the prior art structures to produce applicants' claimed field effect transistor comprising a dielectric layer atop the source drain regions that extends under the sidewalls of the conductive layer, as recited in amended Claim 30. This rejection is thus improper since the prior art does not suggest this drastic modification. The law requires that a prior art reference provide some teaching, suggestion, or motivation to make the modification obvious.

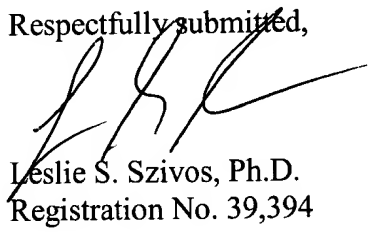
Here, there is no motivation provided in the disclosures of the applied prior art references, or otherwise of record, which would lead one skilled in the art to make the modification mentioned hereinabove. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Fritch, 972 F.2d, 1260,1266, 23 USPQ 1780,1783-84 (Fed. Cir. 1992). There is no suggestion in the prior art of applicants' claimed field effect transistor recited in amended claim 30.

Therefore, all the claims of the present application are not obvious from the prior art applied in the Office Action.

Based on the above amendments and remarks, the §103 rejection has been obviated; therefore reconsideration and withdrawal of the instant §103 rejection is respectfully requested.

Wherefore reconsideration and allowance of the claims of the present application are respectfully requested.

Respectfully submitted,



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